

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. .... 09/651,815  
Priority Filing Date .... August 30, 2000  
 Inventor ..... Jerome Michael Eldridge  
 Assignee ..... Micron Technology, Inc.  
Priority Group Art Unit ..... 2813  
Priority Examiner ..... Laura M. Schillinger  
 Attorney's Docket No. .... MI22-1914  
 Title: Methods for Forming Void Regions, Dielectric Regions and Capacitor Constructions

**PRELIMINARY AMENDMENT**

To: Assistant Commissioner for Patents  
 Washington, D.C. 20231

From: D. Brent Kenady (Tel. 509-624-4276; Fax 509-838-3424)  
 Wells, St. John, Roberts, Gregory & Matkin P.S.  
 601 W. First Avenue, Suite 1300  
 Spokane, WA 99201-3828

**AMENDMENTS****In the Specification**

At page 1, before the "Technical Field" insert the following:

**CROSS REFERENCE TO RELATED APPLICATION**

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/651,815, filed August 30, 2000, entitled "Methods of Forming Void Regions, Dielectric Regions and Capacitor Constructions," naming Jerome Michael Eldridge as inventor, which is a continuation of U.S. Patent Application Serial No. 09/146,117, filed September 2, 1998, now U.S. Patent No. 6,140,200, the disclosure of which is incorporated by reference.

### **In the Claims**

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 C.F.R. § 1.121(c)(1)(i). Cancel all previous versions of any pending claim.

A marked up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 C.F.R. § 1.121(c)(1)(ii). Any claim not accompanied by a marked up version has not been changed relative to the immediate prior version, except that marked up versions are not being supplied for any added claim or canceled claim.

## **CLAIMS**

Cancel claims 1-89 and 97.

90. A method of forming a void region associated with a substrate, comprising:

providing a substrate;

forming a sacrificial mass over the substrate;

forming a layer over the mass; and

subjecting the mass to conditions wherein a component of the mass transports from the mass into the layer to form a mixture of the layer and the component, and wherein transporting the component leaves an enclosed void region between the substrate and the mixture of the layer and the component.

91. The method of claim 90 wherein the layer comprises silicon nitride.

92. A method of forming a void region associated with a substrate, comprising:

providing a substrate;

forming a sacrificial mass over the substrate;

forming a metal-comprising layer over the mass; and

subjecting the mass to conditions which transport a component of the mass to the metal-comprising layer, the transported component being alloyed into the metal-comprising layer and leaving a hermetically-sealed void region between the metal-comprising layer and the substrate.

93. The method of claim 92 wherein less than all of the sacrificial mass is transported to the metal-comprising layer.

94. The method of claim 92 wherein substantially all of the sacrificial mass is transported to the metal-comprising layer.

95. The method of claim 92 wherein the metal-comprising layer comprises one or more of vanadium, zirconium, titanium, tantalum and iron.


97. Cancel.

**REMARKS**

Claims 1-89 and 97 have been canceled without prejudice. Claims 90-96 are pending in the application, and Applicant requests examination of such pending claims.

Respectfully submitted,

Dated: 1-11-02

By:   
D. Brent Kenady  
Reg. No. 40,045

EL84405512

EL169834801

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**APPLICATION FOR LETTERS PATENT**

\* \* \* \* \*

**METHODS OF FORMING VOID REGIONS,  
DIELECTRIC REGIONS AND CAPACITOR  
CONSTRUCTIONS**

\* \* \* \* \*

INVENTOR

Jerome Michael Eldridge

ATTORNEY'S DOCKET NO. MI22-978

Priority Application Serial No. .... 09/651,815  
Priority Filing Date .... August 30, 2000  
Inventor .... Jerome Michael Eldridge  
Assignee .... Micron Technology, Inc.  
Priority Group Art Unit .... 2812  
Priority Examiner .... Laura M. Schillinger  
Attorney's Docket No. .... MI22-1914  
Title: Methods for Forming Void Regions, Dielectric Regions and Capacitor  
Constructions

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING  
PRELIMINARY AMENDMENT

**In the Specification**

The replacement specification paragraphs incorporate the following amendments. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

**CROSS REFERENCE TO RELATED APPLICATION**

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/651,815, filed August 30, 2000, entitled "Methods of Forming Void Regions, Dielectric Regions and Capacitor Constructions," naming Jerome Michael Eldridge as inventor, which is a continuation of U.S. Patent Application Serial No. 09/146,117, filed September 2, 1998, now U.S. Patent No. 6,140,200, the disclosure of which is incorporated by reference.

**In the Claims**

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Claims 1-89 and 97 have been cancelled without prejudice.

**-END OF DOCUMENT-**



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Priority Filing Date ..... August 30, 2000  
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 Attorney's Docket No. .... MI22-1914  
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**INFORMATION DISCLOSURE STATEMENT**

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending Application Serial No. 09/651,815, filed August 30, 2000, upon which the above-identified application relies for a priority date under 35 U.S.C. §120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). As a courtesy, Applicant submits copies of the cited references for review.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 1-11-02



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11/11/02 11:11:11 AM

Form PTO-1449		U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1914		SERIAL NO. Priority 09/651,815	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Jerome Michael Eldridge			
				FILING DATE Priority August 30, 2000		GROUP Priority 2813	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	3,954,523	05/76	Magdo et al			
	AB	5,023,200	06/91	Blewer et al.			
	AC	5,470,801	11/95	Kapoor et al			
	AD	5,885,900	03/99	Schwartz			
	AE	5,731,241	03/98	Jang et al.			
	AF	5,783,253	07/98	Roh			
	AG						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes      No
	AL						
	AM						
	AN						
	AO						
	AP						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc )							
	AQ		Togo, M , "A Gate-side Air-gap Structure (GAS) to Reduce the Parasitic Capacitance in MOSFETs", 1996 Sympos on VLSI Technology				
			Digest of Technical Papers, IEEE 1996, pp. 38-39				
	AR		Anand, M B , "NURA A Feasible, Gas-Dielectric Interconnect Process", 1996 Symposium on VLSI Technology Digest of Technical				
			Papers, IEEE 1996, pp 82-83				
	AS		Watanabe, H , "A Novel Stacked Capacitor with Porous-Si Electrodes for High Density DRAMs", Microelectronics Research				
			Laboratories, NEC Corp. date unknown, pp. 17-18				
	AT		ABSTRACT Anderson, R C et. al., "Porous Polycrystalline Silicon A New Material For MEMS", Jnl. of Microelectromechanical				
			Systems (Mar 1994). Vol 3. No 1, pp. 10-18				
	AU		M B Anand, "Use of Gas as Low-k Interlayer Dielectric in LSI's Demonstration of Feasibility", IEEE Transactions On Electron				
			Devices. Vol 44, No 11, November 1997, pp 1965-1971				
EXAMINER				DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. MI22-1914	SERIAL NO. Priority 09/651,815		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Jerome Michael Eldridge			
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U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	U.S. Patent Application Serial No. 08/947,847		Juengling et al.			10/9/97
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
	AL						
	AM						
	AN						
	AO						
	AP						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc )							
	AQ						
	AR						
	AS						
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PRIORITY FILING DATE ..... August 30, 2000  
INVENTORSHIP ..... Jerome Michael Eldridge  
PRIORITY GROUP ART UNIT ..... 2813  
PRIORITY EXAMINER ..... Laura M. Schillinger  
 ATTORNEY'S DOCKET NO. .... MI22-1914  
 TITLE: Methods for Forming Void Regions, Dielectric Regions and Capacitor  
 Constructions

Assistant Commissioner for Patents  
 Washington, D. C. 20231  
 Attention: Official Draftsman


**SUBSTITUTE DRAWING REQUEST**

Please enter the enclosed formal drawings in the above-referenced  
 application in place of the originally filed drawings. The content of the drawings  
 are identical to those now on file in this application.

Acknowledgment of receipt of the formal drawing sheets and their  
 acceptance into the file is requested.

Respectfully submitted,

Date: 1-11-02

By:   
 D. Brent Kenady  
 Reg. No.: 40,045  
 WELLS, ST. JOHN, ROBERTS,  
 GREGORY & MATKIN P.S.  
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*Enclosures: 4 sheets of Formal Drawings (Figs. 1-8)*